REMARKS

At the time of the Office Action dated September 9, 2004, claims 1-18 were pending, all of which stand rejected.

In this Amendment, claims 1-4 and 6-10 have been amended. Care has been exercised to avoid the introduction of new matter. Specifically, claims 1 and 10 have been amended to clarify the definition of the claimed limitations. Adequate descriptive support for the amendment of claims 1 and 10 can be found in, for example, Fig. 2 and relevant description of the specification. Claims 2-4 and 6-9 have been amended only for better form, but their scopes are not narrowed for any reason relating to patentability.

Specification.

The disclosure has been objected to because of informalities. In response, Applicant has amended the specification, as attached, thereby overcoming the stated bases for the objection to the disclosure. Therefore, withdrawal of this objection is respectfully solicited.

Drawings.

The drawings have also been objected to because according to the Examiner, the configuration regarding claims 6 and 8 is not shown in the drawings. Applicant acknowledges, with appreciation, Examiner Fleming's courtesy and professionalism in conducting a telephonic interview on September 21, 2004, to confirm that "Figure 6 and 8" in paragraph 2 of the Office Action is intended to be --claims 6 and 8--.

In response, Applicant submits that Fig. 10 structurally shows the configuration regarding claims 6 and 8. By referring to the description and Figs. 10 and 13-16, it is understandable that a first processor 11 is configured for performing as a predicting unit and a frequency changing unit, recited in claims 6 and 8. Applicant, therefore, respectfully requests the Examiner to review the drawings, and solicits withdrawal of this objection to the drawings.

Claims 1, 9, 10 and 18 have been rejected under 35 U.S.C. §102(b) as being anticipated by Tatsuhiko (JP05-28116).

In the statement of the rejection, the Examiner asserted that Tatsuhiko discloses a multiprocessor system identically corresponding to what is claimed.

It is established that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicant submits that Tatsuhiko does not disclose a multiprocessor system and a control method of a multiprocessor system including all the limitations recited in claims 1 and 10, as amended, within the meaning of 35 U.S.C. §102.

Tatsuhiko relates to a multiprocessor system intended to improve processing speed and reduce power consumption. In the system, a request count device 2 counts access requests to a shared memory 3 from processors P1 to P3 in each prescribed period of time. Based on the

counting results, frequencies of respective operation clock signals CLK1-CLK3 supplied to processors P1-P3 are variably controlled.

Since Applicant thought that the Examiner might have considered that the claimed "processing time" is equal to how many times a processor accesses the shared memory 3 in each prescribed period of time, as described in Tatsuhiko, claims 1 and 10 have been amended to clarify that limitation. In claims 1 and 10, a "processing time" for a first processor is time necessary to complete first predetermined processing and a "processing time" of a second processor is time necessary to complete second predetermined processing.

Tatsuhiko discloses counting accesses to the shared memory 3 by each processor, but not to disclose the "processing time," as amended. In addition, Tatsuhiko does not explicitly or implicitly disclose that counting accesses to the shared memory 3 means "processing time" necessary to complete predetermined processing. Applicant thus submits that the reference does not disclose that a process is performed based on "a ratio between a processing time of said first processor necessary to complete said first predetermined processing and a processing time of said second processor necessary to complete said second predetermined processing," recited in claims 1 and 10.

Accordingly, Tatsuhiko et al. does not disclose a multiprocessor system and a control method of a multiprocessor system including all the limitations recited in claims 1 and 10, as amended, within the meaning of 35 U.S.C. §102.

It is also noted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 9 and 18 are patentable because they respectively include all the limitations of independent claims 1 and 10.

Therefore, Applicant respectfully solicits withdrawal of the rejection of claims 1, 9, 10 and 18 and favorable consideration thereof.

Claims 2-8 and 11-17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Tatsuhiko in view of Mizuno (JP08-190535).

In the statement of the rejection, the Examiner admitted that Tatsuhiko does not teach the limitations recited in claims 2-8 and 11-17. Then, the Examiner cited Mizuno, asserting that the reference teaches the missing features and concluding that it would have been obvious to modify Tatsuhiko's system based on the teachings of Mizuno.

It is well settled that to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Applicant submits that Tatsuhiko et al. and Mizuno would not have suggested each and every limitation of claims 2-8 and 11-17.

Mizuno discloses a component processor and power distributed multiprocessor. For example, Fig. 1 shows a component processor comprising a processor 101 and a phase lock loop circuit (PLL) 102. When a processing load is large, processor 101 controls PLL 102 to increase a frequency of a clock signal. When a processing load is small, processor 101 controls PLL 102 to reduce the frequency. This component processor is connected to other ones to constitute a multiprocessor.

In response, Applicant submits that as discussed above, Tatsuhiko does not disclose all the limitations recited in claims 1 and 10 upon which claims 2-8 and 11-17 depend. Moreover, Mizuno does not cure the argued fundamental deficiencies of Tatsuhiko. Each component processor disclosed in Mizuno controls a frequency of its clock signal based on its processing load,

independently of a processing load of another component processor. On the other hand, in the claimed invention, "a clock frequency control unit" controls "a frequency of a clock being input to said first processor, according to a ratio between a processing time of said first processor necessary to complete said first predetermined processing and a processing time of said second processor necessary to complete said second predetermined processing" (see claim 1) (emphasis added). Paragraph [0027] of Mizuno discusses how to determine whether a processing load is large or small. The paragraph discloses that the determination is made based on how many times pilot data is outputted from processor 101 (pilot data is outputted when a predetermined batch has been processed). However, it is apparent that the paragraph does not teach the limitations recited in claims 1 and 10, as amended.

Further, Tatsuhiko determines the load state of the processor based on the access requests to the shared memory. In Mizuno, the data amount accumulated in the FIFO buffer is input to the processor via the FIFO monitoring line, to determine the load state of the processor. In either case, special means for monitoring the operation load of the system is necessary. By comparison, in the present invention, the load of each processor is predicted using only the "estimate of the processing time" necessary for the individual processor to complete the processing (see, e.g., claims 1 and 3). The information required is only the "(ratio of) the estimate(s) of the processing time(s)" or prediction as to whether to wait or not, and the existing processor itself carries out the determining process. This eliminates the need of the operation load monitoring means which is necessary for Tatsuhiko and Mizuno.

Applicant notes that the present invention relates to reduction of waiting time for synchronization that would occur in a multiprocessor. In the case where one processor is to operate in cooperation with another processor, if it is known in advance that one of the processors should

wait for synchronization, then the processing is controlled such that the processor that is supposed to wait is made to perform processing slowly. This concept is not found in the prior art where the processor that is currently waiting (or currently low in load) is made to perform processing slowly.

Accordingly, Applicant submits that Tatsuhiko et al. and Mizuno, would not have taught or suggested each and every limitation of claims 2-8 and 11-17. Therefore, withdrawal of the rejection of the claims is respectfully solicited.

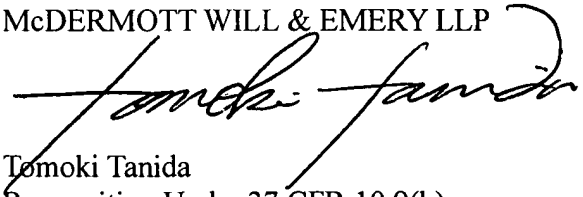
Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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